CLAIMS

1. An active matrix electroluminescent display device comprising an array of display pixels (1), each pixel comprising:

an electroluminescent display element (2);

an amorphous silicon or microcrystalline silicon first drive NMOS transistor (22) connected between the anode of the display element (2) and a power supply line (26);

a storage capacitor (24) between the anode of the display element (2) and the gate of the first drive transistor (22); and

an amorphous silicon or microcrystalline silicon second drive NMOS transistor (30) for supplying a holding voltage to the anode of the display element (2).

2. A device as claimed in claim 1, wherein the second drive transistor (30) is connected between the power supply line (26) and the anode of the display element (2).

3. A device as claimed in claim 1, wherein the second drive transistor (30) is connected between a second power supply line (32) and the anode of the display element (2).

4. A device as claimed in claim 3, wherein the second power supply line (32) is shared between pixels in a row of the array.

5. A device as claimed in any preceding claim, wherein the gate of the first drive transistor (22) is coupled to a data signal line (6) through an address transistor (16).

6. A device as claimed in claim 5, wherein the data signal line (6) comprises a column conductor shared between pixels in a column of the array.

7. A device as claimed in claim 5 or 6, wherein the gate of the address transistor (16) is coupled to a row conductor (4) shared between pixels in a row of the array.

8. A device as claimed in any preceding claim, wherein the first and second drive transistors (22,30) comprise microcrystalline silicon TFTs comprising silicon crystallites of size 40nm – 140nm in an amorphous silicon matrix.

9. A method of driving the pixels of an active matrix electroluminescent display device comprising an array of display pixels (1) each having an electroluminescent display element (2), the method comprising:

holding the voltage across the display element (2) by applying a holding voltage through a first amorphous silicon or microcrystalline silicon NMOS transistor (30), the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor (22);

while holding the voltage across the display element (2), storing a desired gate-source voltage on a storage capacitor (24) connected between the gate and source of the second transistor (22), the gate-source voltage corresponding to a desired source-drain current for driving the display element (2);

removing the holding voltage from the display element (2); and

driving the desired source-drain current through the electroluminescent display element (2).

10. A method as claimed in claim 9, wherein the desired source-drain current is driven through the second transistor (22) by applying a first power supply voltage (26) to the second transistor (22).

11. A method as claimed in claim 10, wherein the first power supply voltage is not applied to the second transistor while the voltage across the display element is held.

12. A method as claimed in claim 11, wherein the first power supply voltage and the holding voltage are provided by a shared power supply line (26).

13. A method as claimed in any one of claims 9 to 12, wherein storing a desired gate-source voltage on a storage capacitor (24) comprises coupling data from a data signal line (6) to the storage capacitor (24) through an address transistor (16).